

IN THE CLAIMS

Listing of Claims:

1. (Previously presented) A method for simulating a model of a chip circuit, comprising method operations of:
 - defining a library of components for a processor;
 - defining interconnections for a set of pipelined processors including the processor, the interconnections defined by analyzing the architectural representation of adjacent processors;
 - generating a processor circuit by combining the library of components and the interconnections for the set of pipelined processors;
 - generating a code representation of a model of the set of pipelined processors;
 - and
 - comparing signals generated by the code representation to signals generated by the processor circuit,
 - wherein if the comparison of the signals is unacceptable, the method includes,
 - generating output for display to identify a cause of the unacceptable comparison of the signals at a block level of the processor circuit.
2. (Original) The method of claim 1, wherein the library of components is included as register transfer logic (RTL).
3. (Original) The method of claim 1, wherein the interconnections for the set of pipelined processors is included in a structural netlist.

4. (Original) The method of claim 1, wherein the set of pipelined processors are configured to manipulate layers of a header of a data packet in stages.

5. (Original) The method of claim 1, wherein the method operation of identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes,

inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals.

6. (Original) A method for debugging a processor circuit, comprising:

identifying a block level location having an error from a first simulation;

inserting a patch into a thread specific to the block level location of the error;

executing the simulation to determine a signal level location of the error through information generated by the patch; and

correcting a code representation of a processor associated with the error.

7. (Original) The method of claim 6, wherein the patch is a print command.

8. (Original) The method of claim 6, wherein the method operation of executing the simulation to determine a signal level location through information generated by the patch includes,

triggering a print statement indicating the signal level location of the error.

9. (Previously presented) An apparatus for simulating a model of a chip circuit, comprising:

a server in which a simulation program logic is stored, the server configured to execute the simulation program logic, wherein the simulation program logic includes:

logic for generating a processor circuit by combining a library of components and defined interconnections for a set of pipelined processors, the interconnections defined by analyzing the architectural representation of adjacent processors;

logic for generating a code representation of a model of the processor; and

logic for comparing signals generated by the code representation to signals generated by the processor circuit,

wherein if the comparison of the signals is unacceptable, the logic for comparing signals includes,

logic for generating output for display to identify a cause of the unacceptable comparison of the signals at a block level of the code representation.

10. (Original) The apparatus of claim 9, wherein logic for identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes,

logic for inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals.

11. (Original) The apparatus of claim 9, wherein the library of components is included as register transfer logic (RTL).

12. (Original) The apparatus of claim 9, wherein the interconnections for the set of pipelined processors is included in a structural netlist.

13. (Original) The apparatus of claim 10, wherein the patch includes logic for executing a print statement.

14. (Original) The apparatus of claim 9, wherein each logic component is one of hardware and software.

15. (Previously presented) A computer readable medium in which program instructions are stored, the program instructions when read by a server of a computing system, cause the server to perform a method for simulating a model of a chip circuit, the method comprising:

defining a library of components for a processor;

defining interconnections for a set of pipelined processors including the processor, the interconnections defined by analyzing the architectural representation of adjacent processors;

generating a processor circuit by combining the library of components and the interconnections for the set of pipelined processors;

generating a code representation of a model of the set of pipelined processors;
and
comparing signals generated by the code representation to signals generated by
the processor circuit,
wherein if the comparison of the signals is unacceptable, the method includes,
generating output for display to identify a cause of the unacceptable
comparison of the signals at a block level of the processor circuit.

16. (Original) The computer readable medium of claim 15, wherein the library of
components is included as register transfer logic (RTL).

17. (Original) The computer readable medium of claim 15, wherein the
interconnections for the set of pipelined processors are included in a structural netlist.

18. (Original) The computer readable medium of claim 15, wherein the set of
pipelined processors are configured to manipulate layers of a header of a data packet
in stages.

19. (Previously presented) The computer readable medium of claim 15, wherein
identifying a cause of the unacceptable comparison of the signals at a block level of
the processor circuit includes,

inserting a patch into the code representation to identify a signal level location
for the unacceptable comparison of the signals.